REMARKS

Claims 1-32 were pending in the present application. Claims 1, 7, 8, 13, 18-21, and 24 have been amended. Accordingly, claims 1-32 remain pending in the application.

Claims 1-32 stand rejected under 35 U.S.C. §103(a) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993) (hereinafter "Liencres") in view of Chandrasekaran et al. (U.S. Patent No. 6,970,872) (hereinafter "Chandrasekaran"). Although Applicant respectfully traverses at least portions of this rejection, Applicant has amended the claims for clarification and to expedite allowance.

Applicant's claim 1, as amended, recites a system comprising in pertinent part

> "a node including an active device, a system memory, and an interface interconnected by an address network and a data network that is separate from the address network;
>
> an additional node coupled to send a coherency message to the interface in the node via an inter-node network, wherein the coherency message requests an access right to a coherency unit;
>
> wherein in response to the coherency message, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet on the address network if the global access state is not the modified state;
>
> wherein in response to the second type of packet, the system memory is configured to send a data packet corresponding to the coherency unit on the data network, regardless of whether the memory has an ownership responsibility for the coherency unit." (Emphasis added)

The Examiner asserts on page 2 in the present Office action "the memory and the active device are part of element 32 in Liencres, which is connected to element 33."

However as shown in FIG. 3a, Liencres clearly shows that the memory alluded to by the Examiner is a cache memory 37, which is not coupled to the bus 33 but to the cache controller 35. In addition, in Applicant's specification and drawings it is clear the claimed memory is a system memory and not a cache memory. Furthermore, even though Liencres clearly shows a system (main) memory coupled by a memory bus 25 to each node, the Examiner has attempted to say the cache memory 37 is analogous to Applicant's claimed memory.

However, although Applicant completely disagrees with this analogy, Applicant has amended the claims to clarify. Thus, Applicant submits element 33 cannot be the address network and the data network as recited in Applicant's claim 1 because it only couples the bus controller 31 to the processor cache controller 35. It does not couple the active device, the interface, and the **system** memory as recited in claim 1.

The Examiner acknowledges Liencres does not teach "wherein in response to the coherency message, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet on the address network if the global access state is not the modified state;" and "wherein in response to the second type of packet, the system memory is configured to send a data packet corresponding to the coherency unit on the data network, regardless of whether the system memory has an ownership responsibility for the coherency unit," as recited in Applicant's claims 1, 13, and 24. However, the Examiner asserts Chandrasekaran teaches the limitations at figure 1 and at col. 2, lines 54-57, col. 2, lines 60-62, and at col. 6, lines 25-36. Applicant respectfully disagrees.

More particularly, the Examiner asserts by ***paraphrasing*** "Chandrasekaran teaches a multi-node network (figure 1) that employs several techniques to reduce latency. One of the methods is called "optimistic read" (col. 2, lines 54-57) where the system sends the read data regardless of whether or not the data is valid (i.e., modified)

(col. 2, lines 60-62). If a request is made its validity is determined. A message is sent granting or denying access to the resource based on its validity. One of the methods of determining validity is "write-time" validity checking (col. 6, lines 25-36). When another node writes out data, it sends out a report stating the latest write time for that data. The read data is invalid once its timestamp comes before the latest write time. The node, now having an invalid read data, will have to request the updated data from the additional node. It would have been obvious... to employ optimistic reading of data using write time validity checking so that reads could be employed when another node has exclusive access but hasn't yet written the data." Applicant respectfully disagrees with the Examiner's application of the Chandrasekaran art to Applicant's claims.

More particularly, Chandrasekaran is directed to optimistic reads and write time validity checking. Taking Chandrasekaran in context Chandrasekaran actually discloses at col. 2 lines 54-67

> "This technique of starting the retrieval of the resource before receiving a response, such as a lock, to a request for permission to access the resource is referred to herein as an "optimistic read." The techniques described herein not only perform an optimistic read but also determine whether the results of the optimistic read are valid, in the sense of providing the correct version of the resource retrieved. If the optimistic read is not valid, then the resource retrieved from the optimistic read is not used. In one embodiment of this aspect, if the version retrieved by the optimistic read is not valid, then another operation is initiated to retrieve the resource, but only after permission is received to access the resource. When the optimistic read results are valid sufficiently often, latency is reduced in retrieving resources." (Emphasis added)

From the foregoing, Applicant submits Chandrasekaran is merely disclosing an optimistic read operation in which the data is retrieved and then checked for validity. This passage does not disclose the system sending the data whether or not it is valid, as suggested by the Examiner. Applicant asserts the Examiner is reading meaning into the passage which does not exist.

In addition, Chandrasekaran discloses at col. 6, lines 25-36

> "In an embodiment using the first type of validity checking, the time that the optimistic read is started is compared to the latest time that the data block was written by any of the other nodes. If the read was started after the last write, the read is valid. **This can be determined even before the read is finished**, but involves the writing node publishing its write time to the other nodes. A node can publish its write time in any way, such as by broadcasting the write time to the other nodes, by storing the write time and responding to requests from other nodes, or by sending the write time to a lock manager. This type of validity checking is called "write-time" validity checking herein." (Emphasis added)

From the foregoing description, Applicant fails to see how this teaches the limitations recited in Applicant's claim 1. Specifically, it appears to Applicant from the above disclosure and from the Examiner's own paraphrasing, that Chandrasekaran is teaching a given node broadcasting or somehow publishing its write time for a write of data. Then some other node does an optimistic read of the data, and if that read occurs earlier in time than the write, the read data would be invalid. The write time may be kept by a lock manager which returns the write validity information. Further, Chandrasekaran discloses that this may be determined even before the read is complete. Thus, Applicant submits this is not the same as the interface sending one type of address packet or a second type of address packet depending on whether the coherency unit in the node is a modified state or not. Further Applicant submits this is not the same as the system memory responding to the second address packet regardless of whether the system memory has an ownership responsibility for the coherency unit.

Thus, Applicant submits neither Liencres nor Chandrasekaran, taken either singly or in combination, teaches or suggests the combination of features recited in Applicant's claim 1.

Accordingly, Applicant submits claim 1, along with its dependent claims patentably distinguishes over Liencres in view of Chandrasekaran for the reasons given above.

Applicant's claims 13 and 24 recite features that are similar to the features recited in claim 1. Thus Applicant submits claims 13 and 24, along with their respective dependent claims, patentably distinguish over Liencres in view of Chandrasekaran for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-94901/SJC.

Respectfully submitted,

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